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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,549	11/24/2003	Shinji Ohuchi	OKI.136D3	1262
20987	7590 07/10/2006		EXAM	
	E FRANCOS, & WHI	LE, THAO X		
ONE FREEDOM SQUARE 11951 FREEDOM DRIVE SUITE 1260			ART UNIT	PAPER NUMBER
RESTON, VA	RESTON, VA 20190			
			DATE MAILED: 07/10/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	10/718,549	OHUCHI ET AL.,				
Office Action Summary	Examiner	Art Unit				
	Thao X. Le	2814				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPL WHICHEVER IS LONGER, FROM THE MAILING D  - Extensions of time may be available under the provisions of 37 CFR 1.1 after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period Failure to reply within the set or extended period for reply will, by statute Any reply received by the Office later than three months after the mailinearned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 136(a). In no event, however, may a reply be tir will apply and will expire SIX (6) MONTHS from the, cause the application to become ABANDONE	N. nely filed the mailing date of this communication. (D (35 U.S.C. § 133).				
Status						
1)⊠ Responsive to communication(s) filed on 31 № 2a)□ This action is <b>FINAL</b> . 2b)⊠ This 3)□ Since this application is in condition for allowa closed in accordance with the practice under €	s action is non-final. ince except for formal matters, pro					
Disposition of Claims						
4) ⊠ Claim(s) 10-20 is/are pending in the application 4a) Of the above claim(s) is/are withdra 5) □ Claim(s) is/are allowed. 6) ⊠ Claim(s) 10-20 is/are rejected. 7) □ Claim(s) is/are objected to. 8) □ Claim(s) are subject to restriction and/or	wn from consideration.					
Application Papers						
9)⊠ The specification is objected to by the Examine 10)⊠ The drawing(s) filed on 28 April 2006 is/are: a Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11)□ The oath or declaration is objected to by the Examine 11.	)⊠ accepted or b)□ objected to drawing(s) be held in abeyance. Se ction is required if the drawing(s) is ob	e 37 CFR 1.85(a). ejected to. See 37 CFR 1.121(d).				
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  a) All b) Some * c) None of:  1. Certified copies of the priority documents have been received.  2. Certified copies of the priority documents have been received in Application No  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  * See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)  1) Notice of References Cited (PTO-892)  2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail D 5) Notice of Informal I 6) Other:					

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#### **DETAILED ACTION**

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### Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 31 May 2006 has been entered.

# Claim Objections

2. Claim 19 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. "the thickness of the semiconductor elements is larger that the thickness of the sealing resin" does not including a narrower range for the thickness.

## Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

<sup>(</sup>a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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- 4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).
- 5. Claims 10, 14-17, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (APA) in view of US 6246010 to Zenner et al.

Regarding claims 10, 19, APA discloses a method of mounting a semiconductor device on a mounting substrate in fig. 9-12 that comprises providing the semiconductor device as including a semiconductor element 1, a sealing resin 4, and a plurality of terminals 3 the semiconductor element 1 having a thickness of 400 µm, fig. 9, a first surface (top) wherein circuitry 2 is formed, a second surface (bottom), and side surfaces positioned between the first and second surfaces, the sealing resin 4 having a thickness between about 100 µm so that the first surface is sealed by the sealing resin 4 and the second and side surfaces are not sealed by the sealing resin 4, fig. 9, each of the plurality of terminals 3 being electrically connected to the circuitry 2; putting the semiconductor device on a mounting substrate, fig. 11, so that the first surface of the

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semiconductor device 1 faces the mounting substrate; and fixing the semiconductor device 1 on the mounting substrate by a heat treatment, specification page 2.

But APA does not disclose a method wherein the semiconductor element

1 having a thickness of 200 microns or less and the sealing resin having a
thickness equal to or greater than half a thickness of the semiconductor element.

However, Zenner discloses a method of mounting a semiconductor device 10 on a mounting substrate 14, fig. 3A, that comprises providing a semiconductor device 10 as including a semiconductor element 12 having a thickness of 20 µm or less, col. 3 line 57 and the sealing resin (adhesive film) having a thickness equal to or greater than half a thickness of the semiconductor element (adhesive film thickness is 2-15 µm), col. 4 line 5. Accordingly, it would have been obvious to one of ordinary skill in art to use the semiconductor element thickness and the adhesive film thickness teaching of Zenner with APA's method because it would have created an extreme high-density electronic package and improved mechanical and thermal properties as taught by Zenner, col. 1 lines 6 and 48-50.

Regarding claims 14-17, Capote discloses that the plurality of terminals are solder balls 14, the heat treatment comprises reflow of solder balls, specification page 2.

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (APA) and US 6246010 to Zenner et al. as applied to claim 10 above and further in view of US 6153448 to Takahashi et al.

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Regarding claim 11, APA discloses the semiconductor element has a central portion and a peripheral portion surrounding the central portion, the peripheral portion, fig. 9

But APA does not disclose the semiconductor device wherein the peripheral portion having a step part, wherein a thickness of the sealing resin on the step part is greater than a thickness of the sealing resin on the central portion.

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However, Takahashi discloses the semiconductor device comprising semiconductor element 1 has a central portion and a peripheral portion surrounding the central portion, the peripheral portion having a step part, fig. 2, wherein a thickness of the sealing resin 12, col. 4 line 67, on the step part is greater than a thickness of the sealing resin on the central portion, fig. 2. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the step part portion teaching of Takahashi with APA's method, because it would have prevented the moisture penetrates from the outside as taught by Takahashi in col. 6 lines 40-45.

7. Claims 12-13, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (APA) and US 6246010 to Zenner et al. as applied to claim 10 above and further in view of US 6297560 to Capote et al.

Regarding claims 12, and 13, APA does not disclose the mounting substrate is printing board.

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However, Capote discloses the method comprises a semiconductor element 10 and mounting substrate 20 is a printing board, col. 1 lines 63-67. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the teaching of Capote with APA, because such mounting substrate is typical for mounting the IC in the flip-chip.

Regarding claim 18, APA does not discloses the method wherein after said fixing, a gap exists between the semiconductor device and the mounting substrate, which are separated by the terminals.

However, Capote discloses the method wherein after said fixing, a gap exists between the semiconductor device and the mounting substrate, which are separated by the terminals, fig. 3. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the teaching of Capote with APA's method, because it would have eliminated the conventional capillary low under-fill process as taught by Capote, see abstract.

#### Response to Arguments

8. Applicant's arguments with respect to claims 10-20 have been considered but are moot in view of the new ground(s) of rejection.

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### Conclusion

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9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le 06 July 2006